What is claimed is:

1. An apparatus for inter alia processing a series of data values V_1 to V_X where data value V_m, for each integer m from 1 to x, corresponds to a complex number A_m+jB_m, where $j = \sqrt{-1}$, with a 2^N bit binary value, where N is an integer greater than 1, to produce a series of data values V'_1 to V'_y where data value V'_p, for each integer p from 1 to y, corresponds to a complex number $A'_p+ jB'_p$, comprising:

a real component shift register R_R and an imaginary component shift register R_I;

each register having a series of 2^N locations Ci for each integer i from 1 to 2^N;

each register associated with a real component adder circuit RA_R, RA_I, respectively, and an imaginary component adder circuit IA_R, IA_I, respectively;

each adder circuit having a series of 2^{N-1} selectively controllable inputs I_k, for each integer k from 1 to 2^{N-1};

the real component adder circuit RA_R coupled with the register R_R such that input I_k receives data from register location C2k-1, for each integer k from 1 to 2^{N-1};

the imaginary component adder circuit IA_R coupled with the register R_R such that input I_k receives data from register location C2k, for each integer k from 1 to 2^{N-1};

the real component adder circuit RA_I coupled with the register R_I such that input I_k receives data from register location C2k, for each integer k from 1 to 2^{N-1};

the imaginary component adder circuit IA_I coupled with the register R_I such that input I_k receives data from register location C2k-1, for each integer k from 1 to 2^{N-1};

each input controllable via a control bit associated with each register location, where the control bits collectively correspond to the 2^N bit binary value and each control bit B_i associated with a location Ci of register R_R is the same as the control bit B_i associated with corresponding location Ci of register R_I for each integer i from 1 to 2^N, such that the input

receives data from the location to which it coupled as a value or an inverse value of the received data, dependent upon the value of the control bit;

each adder circuit having an output for outputting the sum of the values received by its respective controllable inputs;

a real component combiner circuit coupled to the outputs of the real component adder circuits RA_R, RA_I for outputting a combined real component value A'_p of a processed value V'_p;

an imaginary component combiner circuit coupled to the outputs of the imaginary component adder circuits IA_R, IA_I for outputting a combined imaginary component value jB'_p of a processed value V'_p; and

said registers R_R, R_I operable to shift the data of respective locations Ci-1 to locations Ci for each integer i from 2 to 2^N and receive new data in location C1 to thereafter generate a next processed value V'_{p+1}.

2. An apparatus according to claim 1 that processes received CDMA communication data where the series of data values V_1 to V_X represent channel response values of a communication signal that has a spreading factor of 2^M where M is a positive integer $\leq$ N, the 2^N bit binary value represents a channel code value associated with the communication signal, and series of data values V'_1 to V'_y represents a row of values of a system transmission coefficient matrix, further comprising:

a control circuit that operatively controls the registers and adder circuits based on the spreading factor of a communication corresponding to the data value series to be processed;

said control circuit operative to sequentially input the series of data values V_1 to V_X followed by a series of 2^N–1 zero values to the registers 2^{N-M} times to produce 2^{N-M}

series of data values V'_1 to V'_y, where $y = x + 2^N-1$, each representing a row of values of the system transmission coefficient matrix; and

said control circuit operative to selectively enable and disable the inputs of the adder circuits when $2^M < 2^N$ such that each time the series of data values V_1 to V_X is input to the registers, a different set of 2^M inputs are enabled from each register with all other adder inputs being disabled.

3. An apparatus according to claim 2 wherein N=4 so that each register has sixteen locations and wherein each adder circuit has eight inputs and a tree of seven adders.

4. An apparatus according to claim 2 wherein each adder circuit comprises a tree of $2^{N-1}-1$ adders.

5. An apparatus according to claim 4 wherein the register location data are binary values and each adder circuit input comprises a selectively operable two's complement circuit that receives a value from the inputs corresponding register location and outputs to the adder tree the received value if the corresponding control bit is one or the two's complement of the received value if the control bit is zero.

6. An apparatus according to claim 5 wherein:

the real component combiner circuit includes a subtracter for subtracting the value of the output of the real component adder circuit RA_R that is coupled with the real component register R_R, from the value of the output of the real component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce the combined real component value; and

the imaginary component combiner circuit includes:

an adder for adding the value of the output of the imaginary component adder circuit IA_R that is coupled with the real component register R_R, with the value of the output of the imaginary component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce a sum value; and

a two's complement circuit coupled to the adder to receive the sum value and produce a two's complement thereof as the combined imaginary component value.

7. An apparatus according to claim 1 wherein each adder circuit comprises a tree of $2^{N-1}-1$ adders.

8. An apparatus according to claim 7 wherein the register location data are binary values and each adder circuit input comprises a selectively operable two's complement circuit that receives a value from the inputs corresponding register location and outputs to the adder tree the received value if the corresponding control bit is one or the two's complement of the received value if the control bit is zero.

9. An apparatus according to claim 8 wherein:

the real component combiner circuit includes a subtracter for subtracting the value of the output of the real component adder circuit RA_R that is coupled with the real component register R_R, from the value of the output of the real component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce the combined real component value; and

the imaginary component combiner circuit includes:

an adder for adding the value of the output of the imaginary component adder circuit IA_R that is coupled with the real component register R_R, with the value of the output of the imaginary component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce a sum value; and

a two's complement circuit coupled to the adder to receive the sum value and produce a two's complement thereof as the combined imaginary component value.

10. A method for inter alia processing a series of data values V_1 to V_x where data value V_m, for each integer m from 1 to x, corresponds to a complex number A_m+jB_m, where $j = \sqrt{-1}$, with a 2^N bit binary value, where N is an integer greater than 1, to produce a series of data values V'_1 to V'_y where is data value V'_p, for each integer p from 1 to y, corresponds to a complex number $A'_p+ jB'_p$, comprising:

providing a real component shift register R_R and an imaginary component shift register R_I; each register having a series of 2^N locations Ci for each integer i from 1 to 2^N, each location has a zero value as its initial content; each register each associated with a real component adder circuit RA_R, RA_I, respectively, and an imaginary component adder circuit IA_R, IA_I, respectively; each adder circuit having a series of 2^{N-1} selectively controllable inputs I_k, for each integer k from 1 to 2^{N-1} the real component adder circuit RA_R coupled with the register R_R such that input I_k receives data from register location C2k-1, for each integer k from 1 to 2^{N-1}; the imaginary component adder circuit IA_R coupled with the register R_R such that input I_k receives data from register location C2k, for each integer k from 1 to 2^{N-1}, the real component adder circuit RA_I coupled with the register R_I such that input I_k receives data from register location C2k, for each integer k from 1 to 2^{N-1}, the imaginary component adder circuit IA_I coupled with the register R_I such that input I_k receives data from register location C2k-1, for each integer k from 1 to 2^{N-1}, each input

controllable via a control bit associated with each register location, where the control bits collectively correspond to the 2^N bit binary value and each control bit B_i associated with a location Ci of register R_R is the same as the control bit B_i associated with corresponding location Ci of register R_I for each integer i from 1 to 2^N, such that the input receives data from the location to which it coupled as a value or an inverse value of the location's content dependent upon the value of the control bit; each adder circuit having an output for outputting the sum of the values received by its respective controllable inputs; a real component combiner circuit coupled to the outputs of the real component adder circuits RA_R, RA_I for outputting a combined real component value; and an imaginary component combiner circuit coupled to the outputs of the imaginary component adder circuits IA_R, IA_I for outputting a combined imaginary component value; and

sequentially processing each data value V_m by shifting the contents of respective locations Ci-1 to locations Ci for each integer i from 2 to 2^N, receiving the real component A_m as the new contents of location C1 of real register R_R, and receiving the imaginary component B_m as the new contents of location C1 of imaginary register R_I, whereby processed values V'_p are produced corresponding to the complex number $A'_p + jB'_p$, where A'_p is a combined real component value output by the real component combiner circuit and jB'_p is a combined imaginary component value output by the imaginary component combiner circuit.

11. A method according to claim 10 that processes received CDMA communication data where the series of data values V_1 to V_X represent channel response values of a communication signal that has a spreading factor of 2^M where M is an integer $\leq$ N, the 2^N bit binary value represents a channel code value associated with the

communication signal, and series of data values V'_1 to V'_y represents a row of values of a system transmission coefficient matrix, further comprising:

sequentially inputting the series of data values V_1 to V_X followed by a series of 2^N–1 zero values to the registers 2^{N-M} times to produce 2^{N-M} series of data values V'_1 to V'_y, where $y = x + 2^N-1$, each representing a row of values of the system transmission coefficient matrix; and

selectively enabling and disabling the inputs of the adder circuits when $2^M < 2^N$ such that each time the series of data values V_1 to V_X is input to the registers, a different set of 2^M inputs are enabled from each register with all other adder inputs being disabled.

12. A method according to claim 11 wherein processing includes:

subtracting the value of the output of the real component adder circuit RA_R that is coupled with the real component register R_R, from the value of the output of the real component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce the combined real component value; and

adding the value of the output of the imaginary component adder circuit IA_R that is coupled with the real component register R_R, with the value of the output of the imaginary component adder circuit RA_I that is coupled with the imaginary component register R_R, to produce a sum value and producing a two's complement thereof as the combined imaginary component value.

13. An apparatus for inter alia processing a series of dual element data values V_1 to V_X where data value V_m, for each integer m from 1 to x, corresponds to a first element A_m and a second element B_m, with a N bit binary value, where N is a positive even integer,

to produce a series of data values V'_1 to V'_y where data value V'_p, for each integer p from 1 to y, corresponds to a first element A'_p and a second element B'_p, comprising:

a first element shift register R_1 and a second element shift register R_2;

each register R_1,R_2 having a series of N locations Ci for each integer i from 1 to N;

each register R_1,R_2 associated with a first component adder circuit $A_{1,1}$, $A_{1,2}$, respectively, and a second component adder circuit $A_{2,1}$, $A_{2,2}$, respectively;

each adder circuit having a series of N/2 selectively controllable inputs I_k, for each integer k from 1 to N/2;

each adder circuit input coupled with a different register location to receive data therefrom;

each adder circuit input controllable via a control bit associated with its respective register location, where the control bits collectively correspond to the N bit binary value and each control bit B_i associated with a location Ci of register R_R is the same as the control bit B_i associated with corresponding location Ci of register R_I for each integer i from 1 to N, such that the input receives data from the location to which it coupled as a value or an inverse value of the received data, dependent upon the value of the control bit;

each adder circuit having an output for outputting the sum of the values received by its respective controllable inputs;

a first component combiner circuit coupled to the outputs of the first component adder circuits $A_{1,1}$, $A_{1,2}$ for outputting a first element value A'_p of a processed value V'_p;

a second component combiner circuit coupled to the outputs of the second component adder circuits $A_{2,1}$, $A_{2,2}$ for outputting a second element value B'_p of a processed value V'_p; and

said registers R_R, R_I operable to shift the data of their respective locations and receive new data to thereafter generate a next processed value V'_{p+1}.

14. The apparatus according to claim 13 wherein:

the first component adder circuit $A_{1,1}$ is coupled with the register R_1 such that input I_k receives data from register location C2k-1, for each integer k from 1 to N/2;

the second component adder circuit $A_{2,1}$ is coupled with the register R_1 such that input I_k receives data from register location C2k, for each integer k from 1 to N/2;

the first component adder circuit $A_{1,2}$ is coupled with the register R_2 such that input I_k receives data from register location C2k, for each integer k from 1 to N/2;

the second component adder circuit $A_{2,2}$ is coupled with the register R_2 such that input I_k receives data from register location C2k-1, for each integer k from 1 to N/2; and

said registers R_1, R_2 are operable to shift the data of respective locations Ci-1 to locations Ci for each integer i from 2 to N and receive new data in location C1 to thereafter generate the next processed value.

15. An apparatus according to claim 14 that processes received CDMA communication data where the series of data values V_1 to V_X represent channel response values of a communication signal that has a spreading factor of 2^M where M is an integer and $2^M \leq N$, the N bit binary value represents a channel code value associated with the communication signal, and series of data values V'_1 to V'_y represents a row of values of a system transmission coefficient matrix, further comprising:

a control circuit that operatively controls the registers and adder circuits based on the spreading factor of a communication corresponding to the data value series to be processed;

said control circuit operative to sequentially input the series of data values V_1 to V_X followed by a series of N-1 zero values to the registers $N/2^M$ times to produce $N/2^M$ series

of data values V'_1 to V'_y, where $y = x + N-1$, each representing a row of values of the system transmission coefficient matrix; and

said control circuit operative to selectively enable and disable the inputs of the adder circuits when $2^M < N$ such that each time the series of data values V_1 to V_X is input to the registers, a different set of 2^M inputs are enabled from each register with all other adder inputs being disabled.